Project Research — Development of a Supply/Demand Infrastructure for Next-generation Electric Power

Low-loss Power Semiconductor

Background and Objective

The development of high-efficiency and compact semiconductor power conversion equipment is a common technical issue regarding the power control of plug-in hybrid or electric cars, IH cooking heaters, heat pump hot-water systems, and power transmission/distribution systems. The wide range practical use of SiC power semiconductor devices, which can realize loss reduction and higher withstanding voltage compared to conventional Si power devices, is expected to contribute toward solving the common issues.

This project aims at the development of technologies for the production of high-quality SiC crystals and the performance improvement of high-voltage devices.

Main results

1 Optimization of the Defect Reduction Process

Thick and high-purity single-crystal SiC films (epilayers) with a long carrier lifetime are essential to realize high-voltage and low-loss SiC switching devices (SiC-IGBT*1). We obtained thick SiC epilayers (up to 140 μm) and a low nitrogen doping concentration (3×10^{14} cm^{-3}) corresponding to a withstanding voltage of 13 kV, which can be adapted to high-voltage power systems, and applied the original defect reduction process named "C-ion implantation and annealing process"[1,2] to the epilayer with different conditions. This post-growth process eliminates carbon vacancy-type point defects and improves carrier lifetimes, and is proven to be able to eliminate defects below the detection limit throughout the volume of the epilayers more than 100 μm from the surface by adjusting the annealing temperature to 1600°C. As the result, we succeeded in enhancing the carrier lifetimes from 2 μs (before the process) to 12.8 μs (after the process) in excess of the requirement values of 5–10 μs for the 13 kV devices (Fig. 1).

2 Development of Defect Conversion Techniques

We clarified that the dislocations (basal plane dislocations: BPDs) causing the degradation of the current conduction performance of SiC bipolar devices such as IGBT*1 are reduced by high-temperature annealing in Ar ambience. This is a new method to convert BPDs to other-type dislocations (threading edge dislocations: TEDs) having no negative impact on the degradation, and we confirmed the conversion of the tip of BPDs to TEDs by synchrotron X-ray topography (Fig. 2)[3]. We also developed a three-dimensional topography technique using a synchrotron X-ray micro beam as a new method to observe dislocations in SiC epilayers to make it possible to optimize the dislocation conversion process and to clarify the conversion mechanism. We succeeded in obtaining three-dimensional images of the BPD-TED conversion points (Fig. 3).

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*1 IGBT: Insulated gate bipolar transistor

Related Patent Submissions and Papers

1 Patent submission 2008-53667, Methods to improve the quality of SiC crystals and SiC devices
2 L. Storasta and H. Tsuchida, Applied Physics Letters 90, 062116 (2007)
3 Patent submission 2011-118419, Production methods of SiC substrates and SiC wafers and SiC semiconductor devices

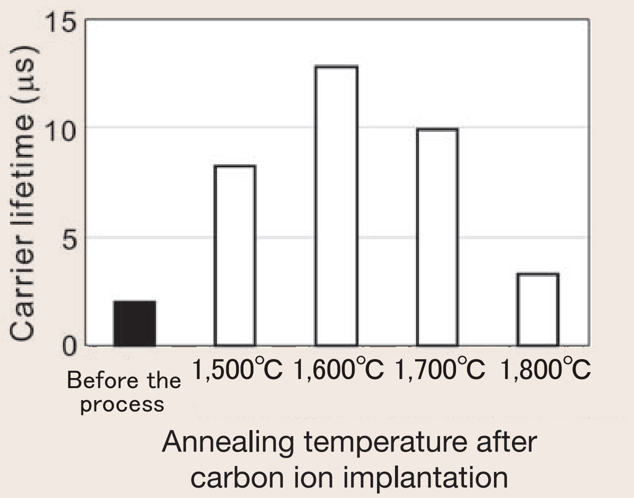

Fig. 1: Changes in the carrier lifetimes of SiC epilayers before and after the carbon ion implantation and annealing process with different annealing temperatures

Carrier lifetimes express the decay times of excess electrons and holes to become the thermal equilibrium, and a longer carrier lifetime achieves low-loss current conduction.

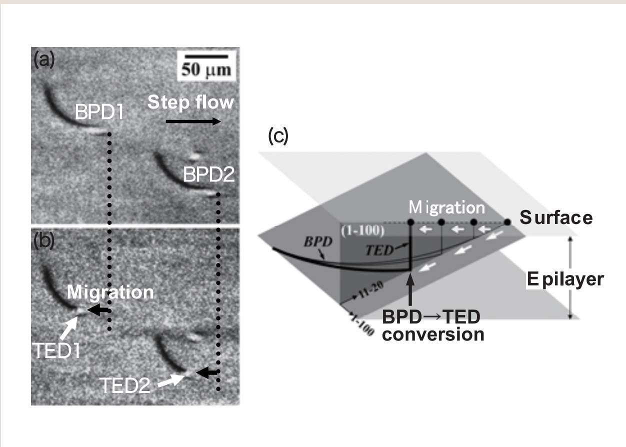

Fig. 2: Conversion of BPDs to TEDs by high-temperature annealing

Synchrotron X-ray topography images of a SiC epilayer (a) before and (b) after 1800°C annealing, showing the conversion of the BPD tips to TEDs; (c) schematic drawing of BPD-TED conversion by high-temperature annealing.

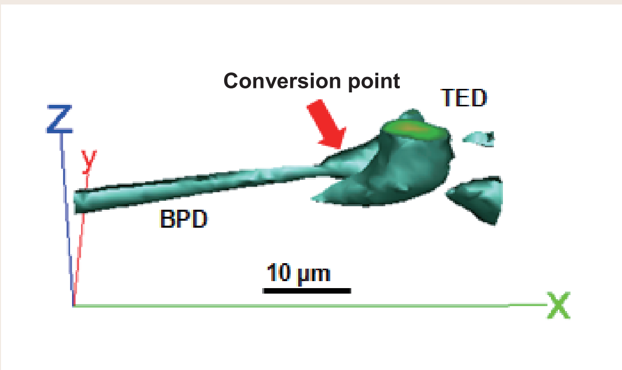

Fig. 3: Three-dimensional synchrotron X-ray topography image taken for a position of BPD-TED conversion

The three-dimensional observation of a BPD-TED conversion is possible by making a side-view of a synchrotron X-ray topography image.